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10071145-020602

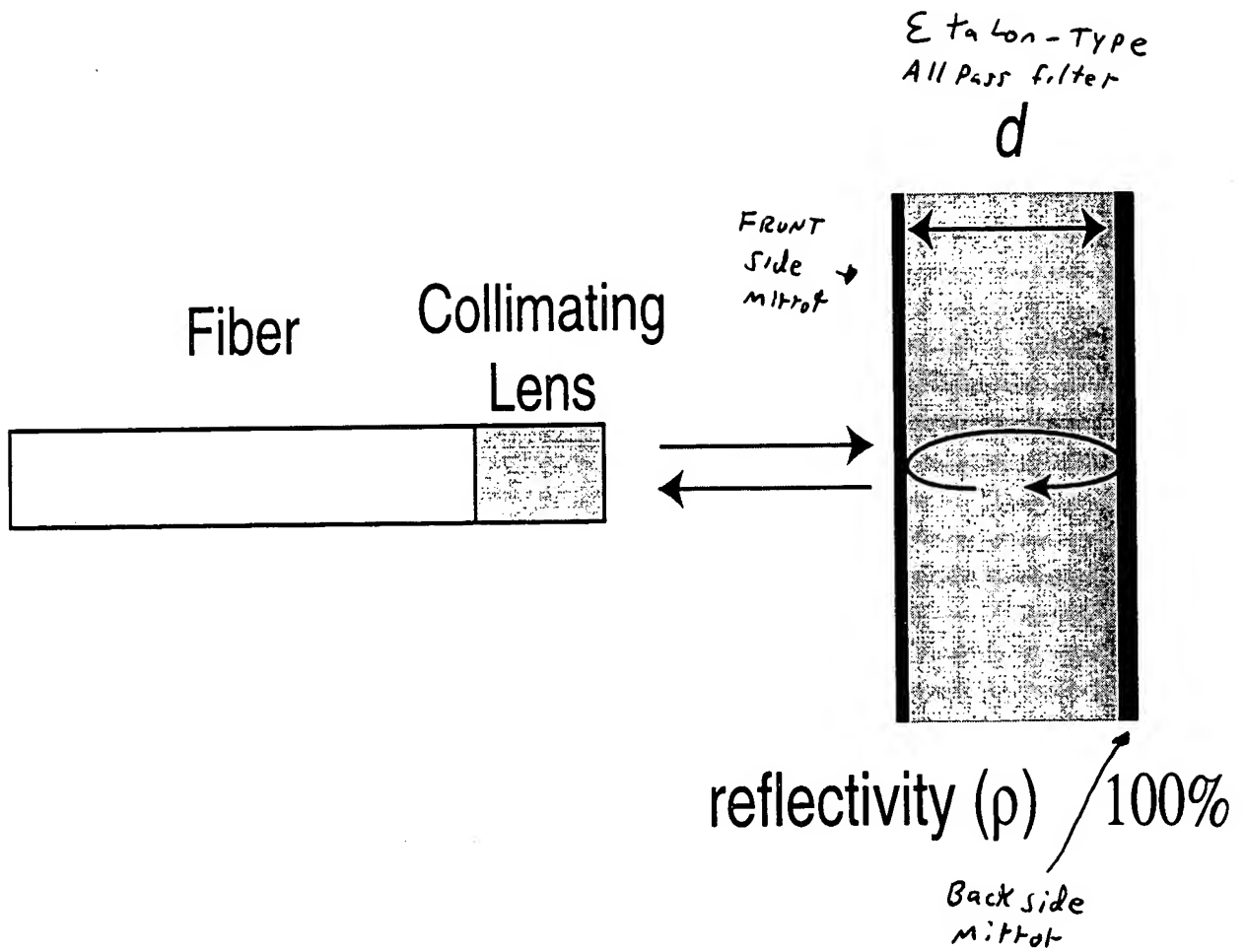


Figure 1

10071145-020602

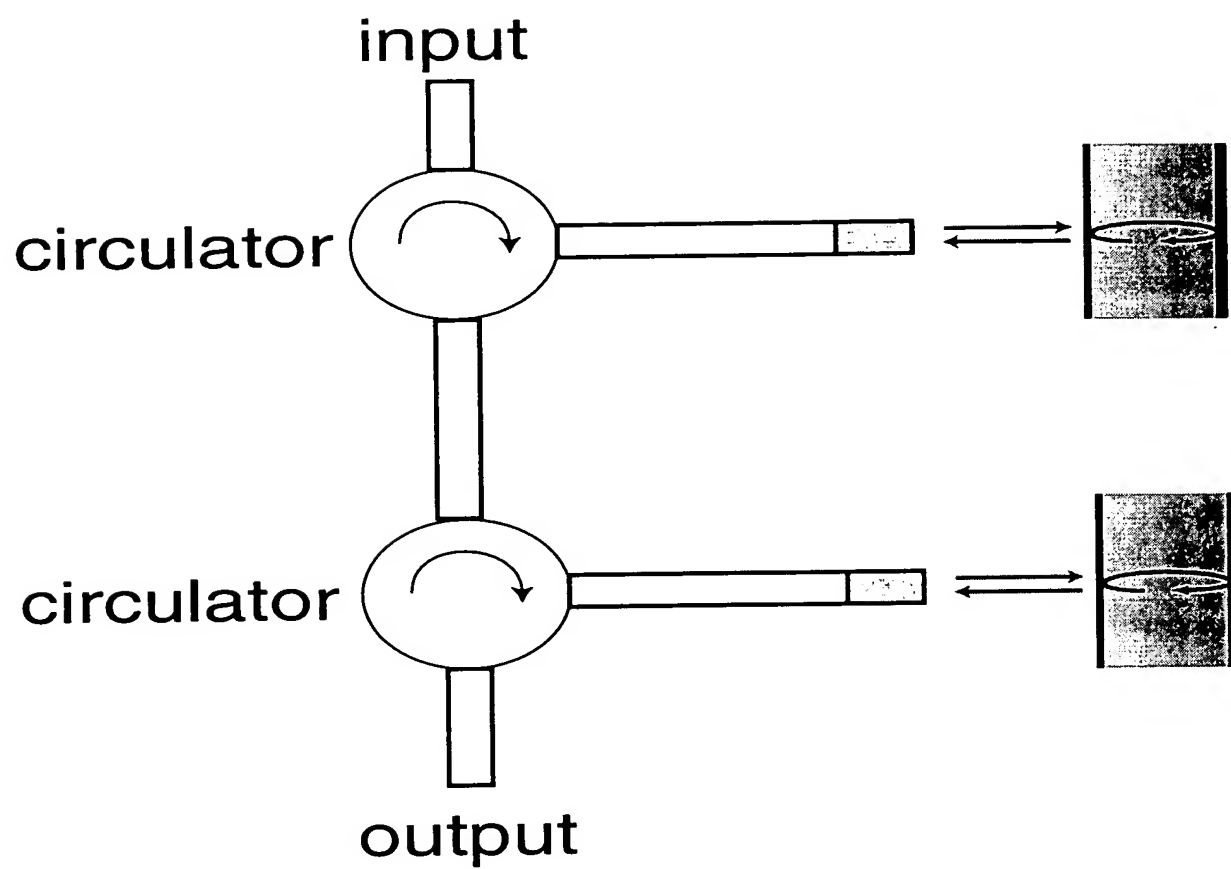


Figure 2

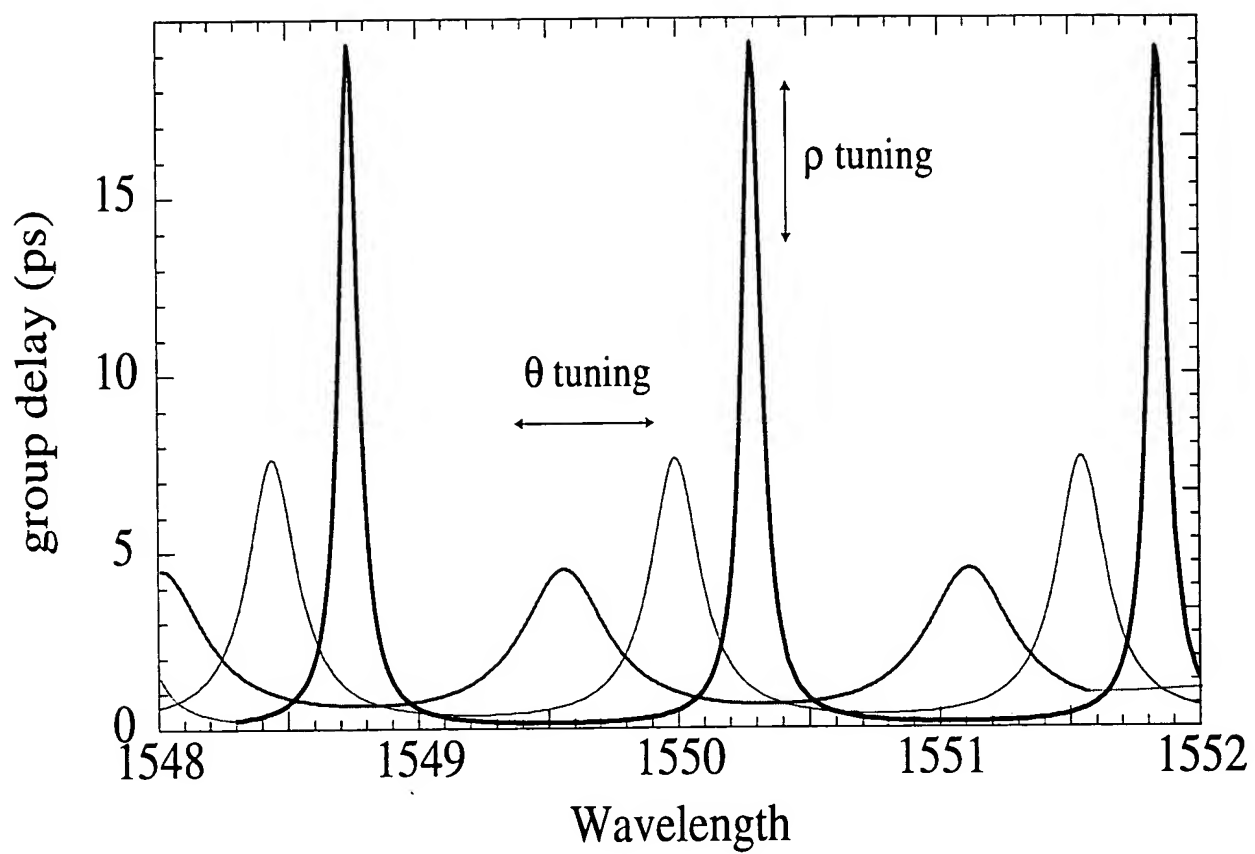


Figure 3

209020" 5477/00F

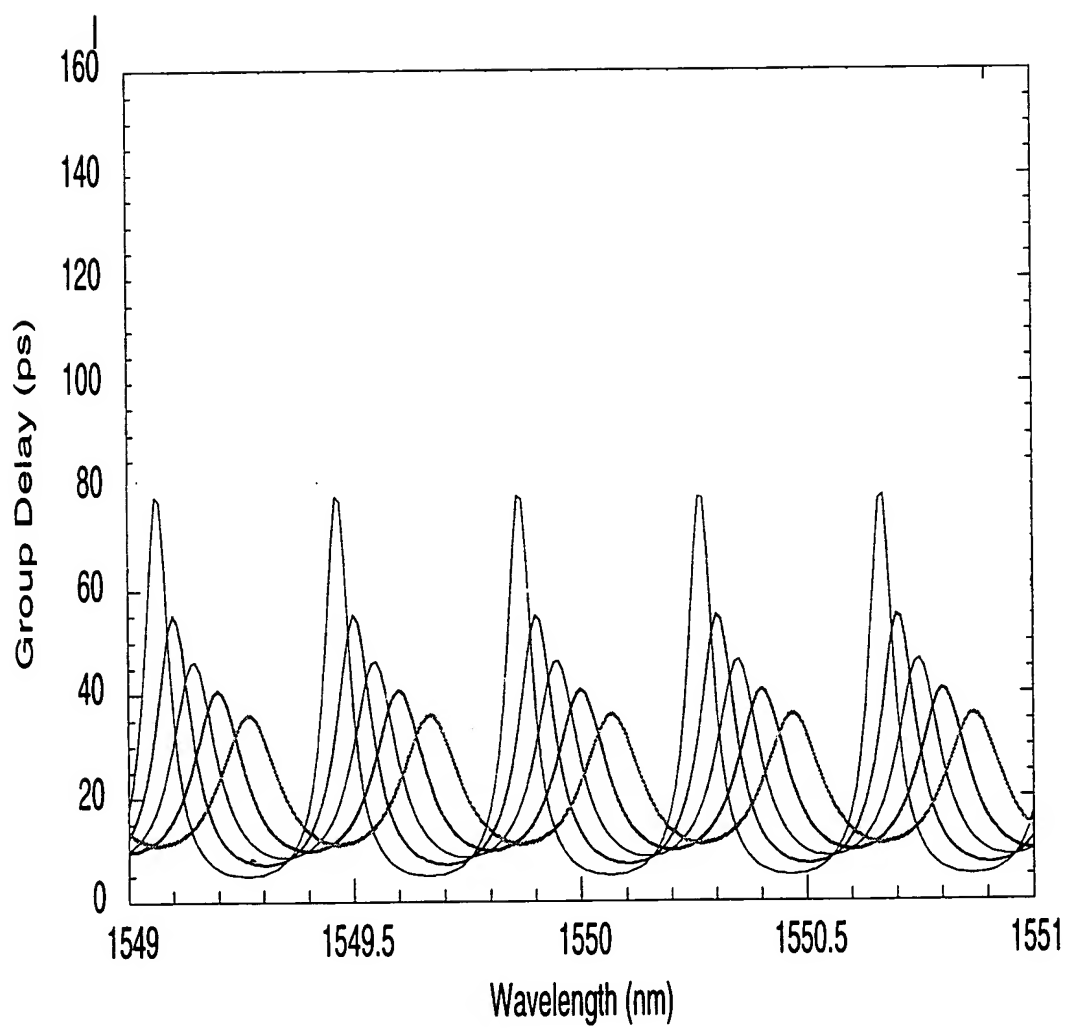


Figure 4

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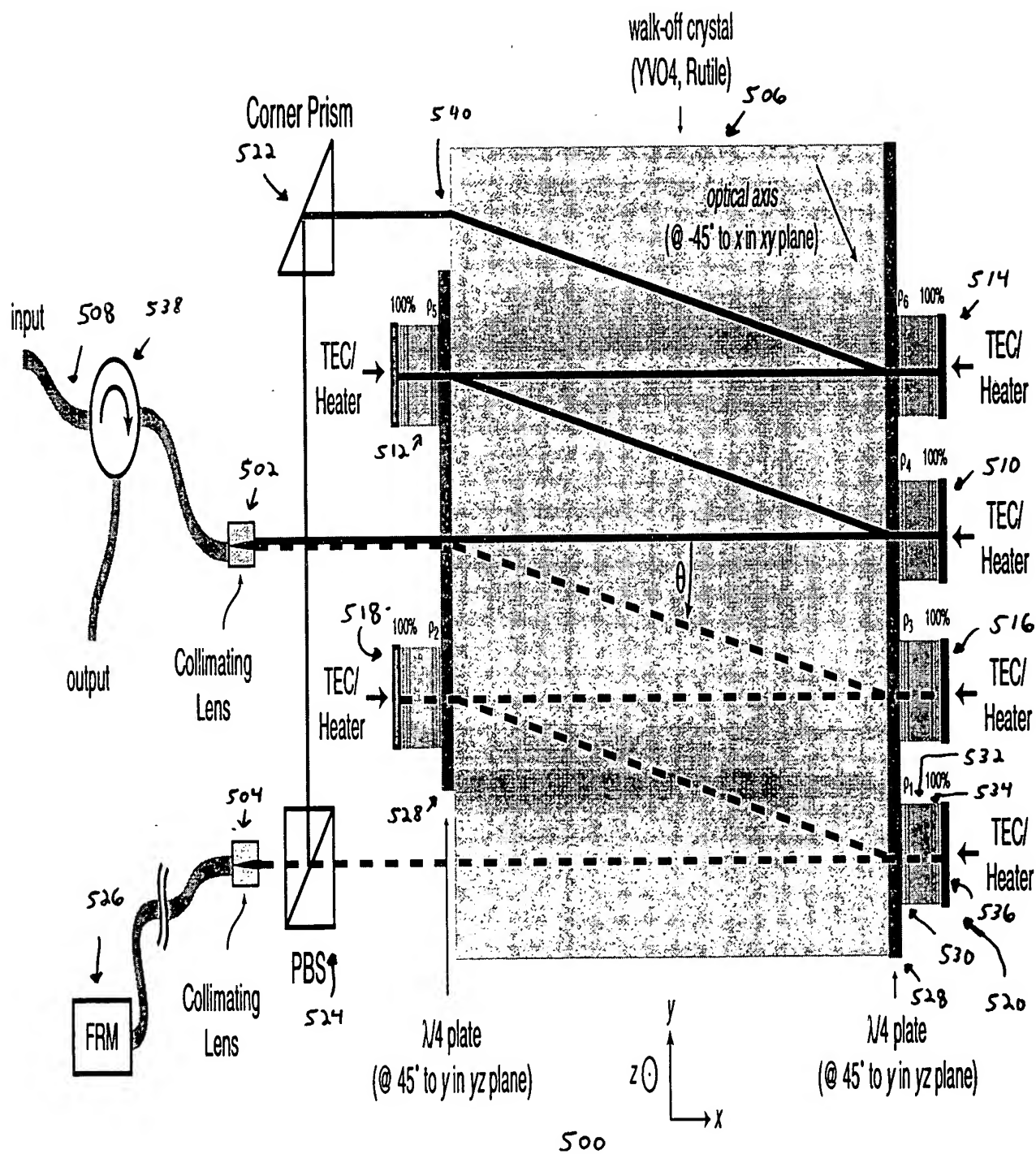


Figure 5

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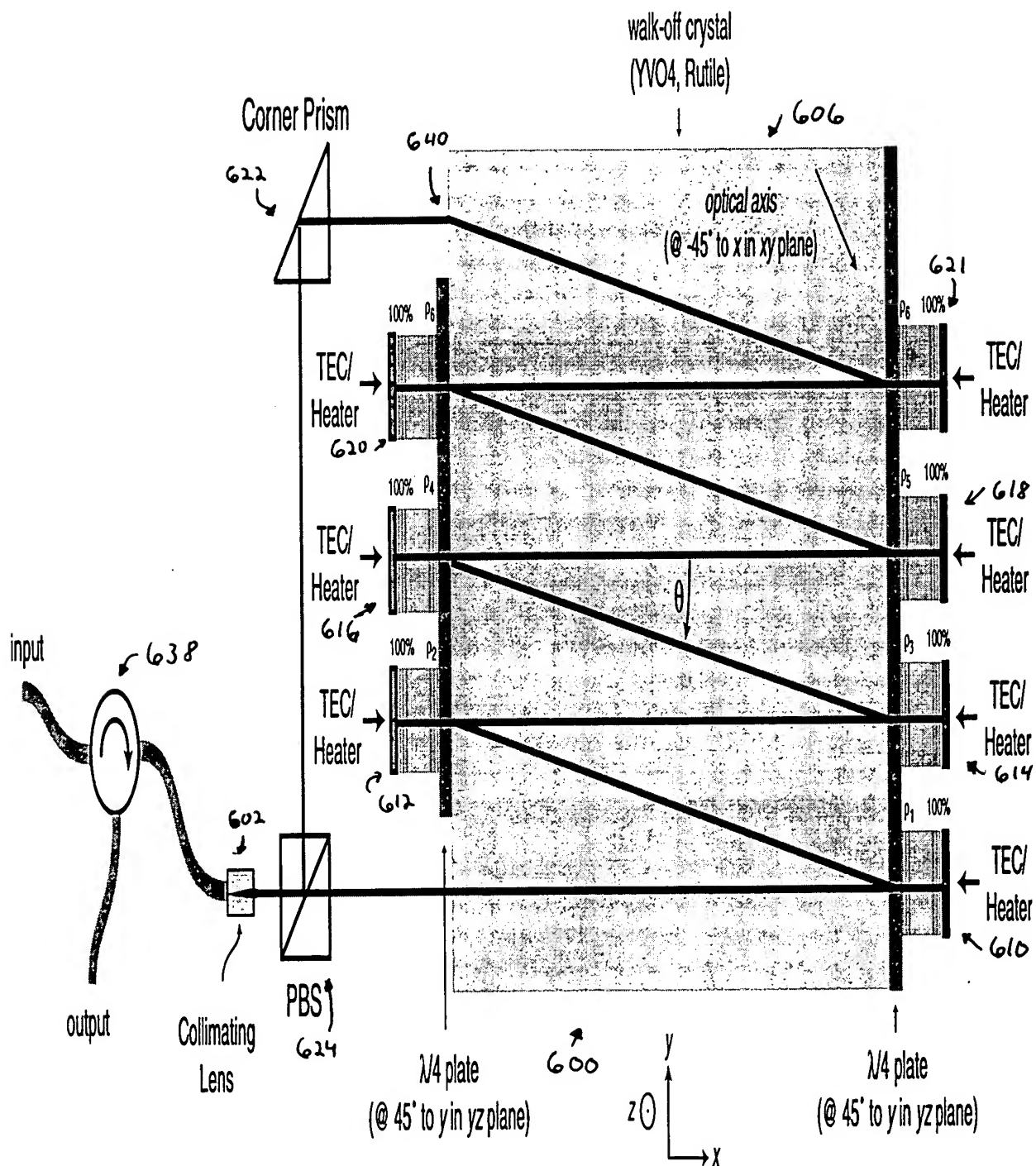


Figure 6

2092020 "SHTT" 001

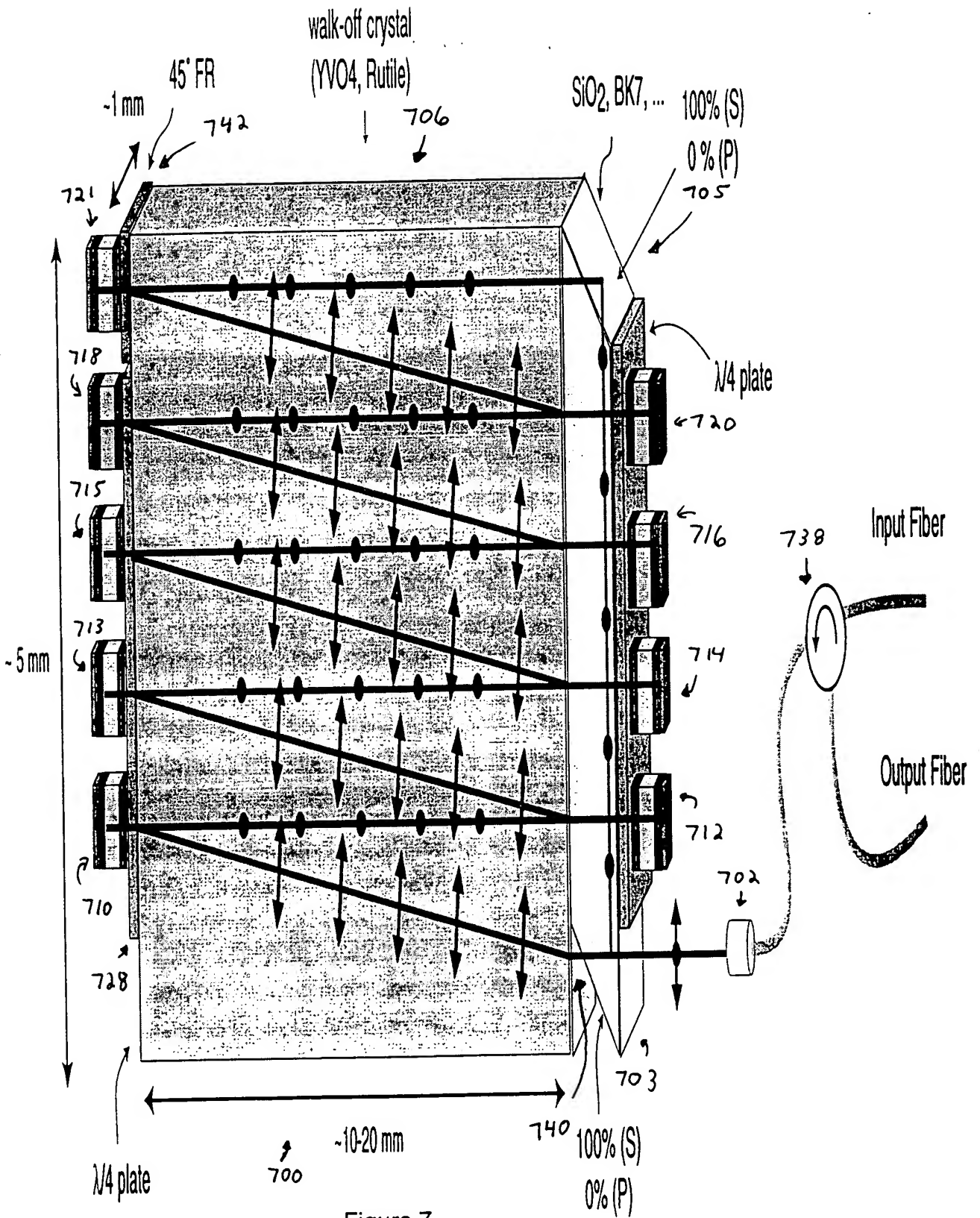


Figure 7

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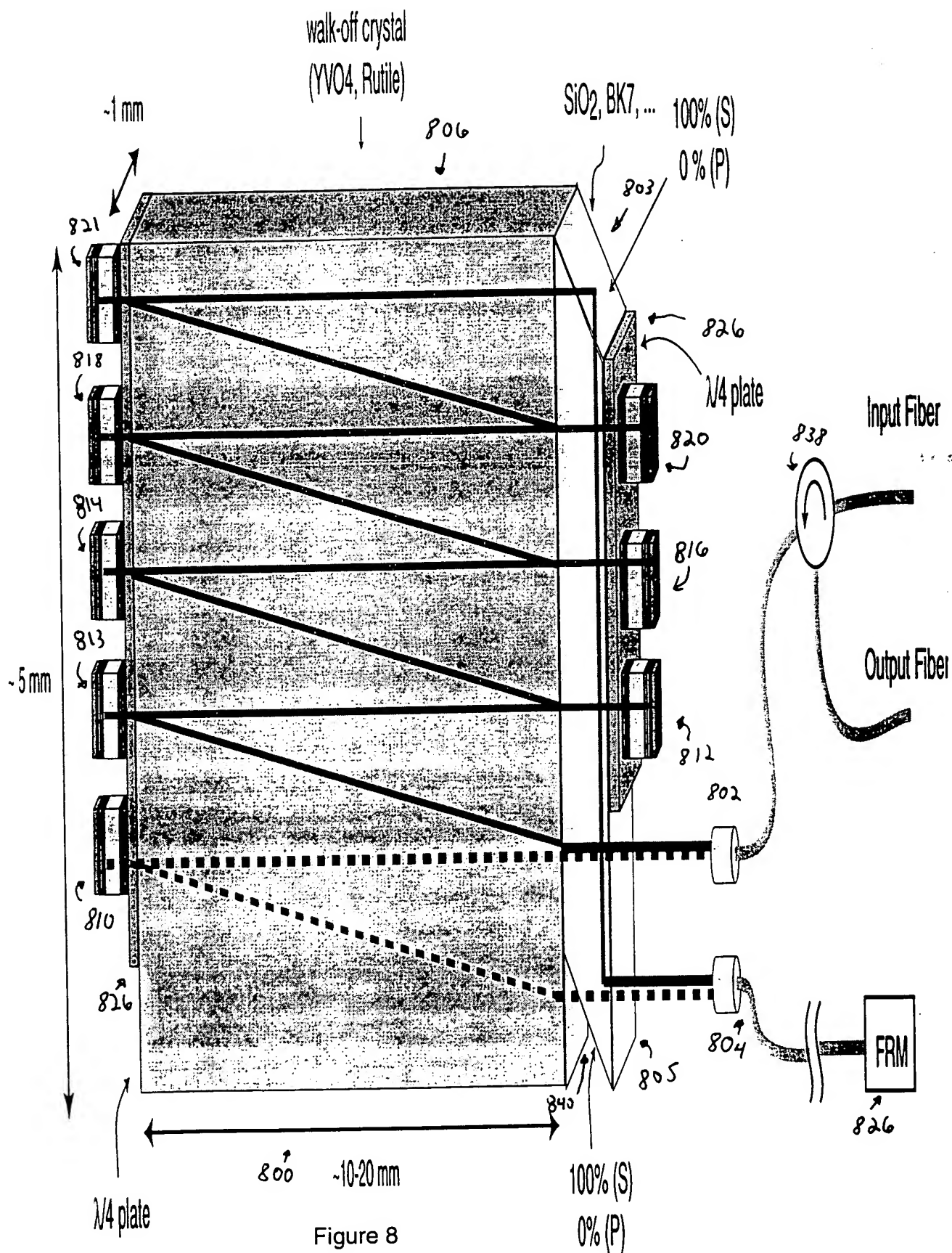


Figure 9 is a schematic diagram of a quantum device, likely a quantum memory or a quantum processor, consisting of five parallel channels. Each channel is defined by a top waveguide (910-914) and a bottom waveguide (912-916), separated by a central region (918-920). The top waveguides are connected to a common input/output line (902-904) via collimating lenses (938) and waveguide sections (934). The bottom waveguides are connected to a common input/output line (900) via collimating lenses (926) and waveguide sections (928). The central region contains five PBS (Polarizing Beam Splitter) elements (950-958) and five $\lambda/4$ plates (928) oriented at 45° to the z-axis in the xz plane. The device is controlled by five TEC/Heater elements (913-919) and five TEC/Heater elements (914-920). A coordinate system (x, y, z) is shown at the bottom right.

209020" 54T 2007

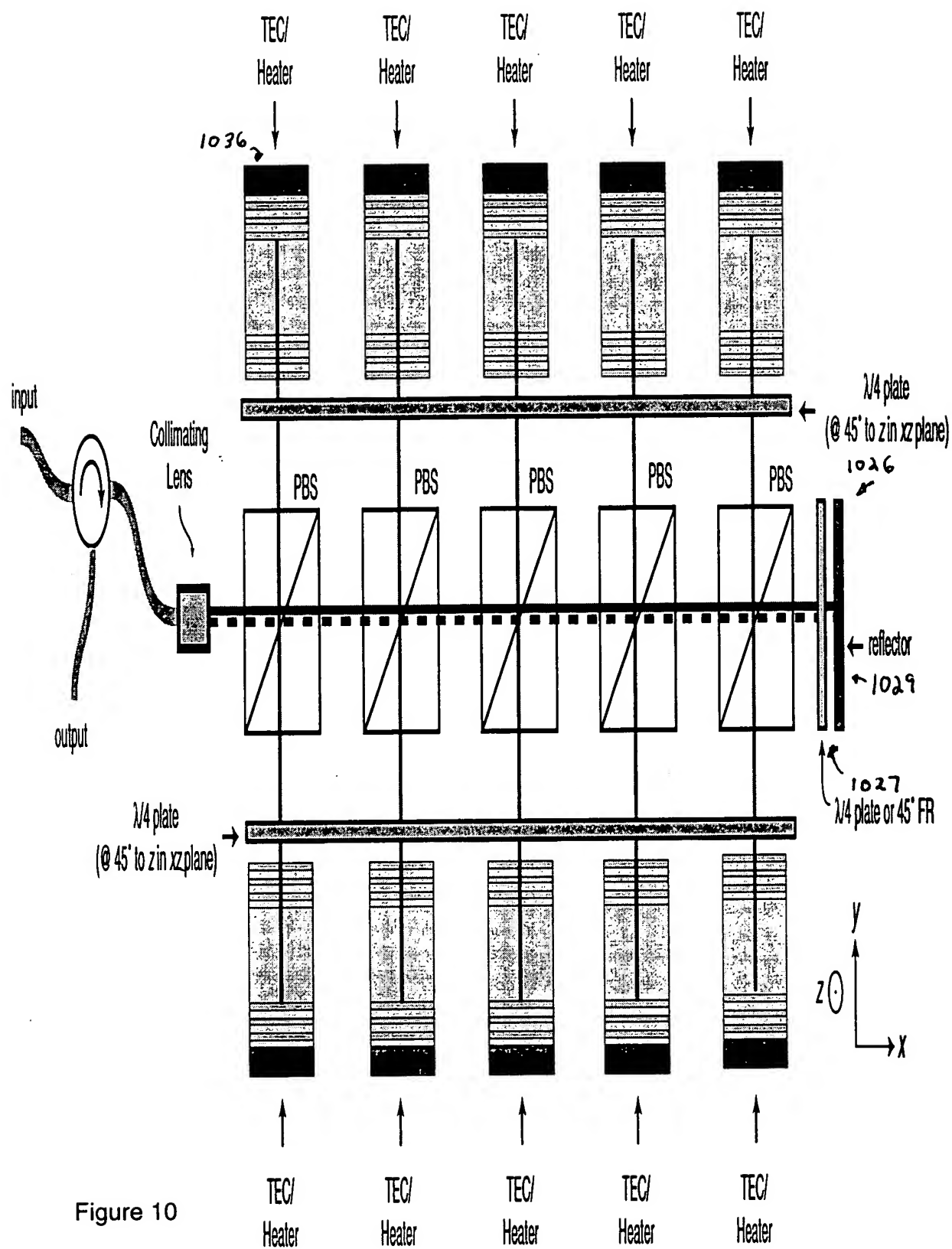


Figure 10

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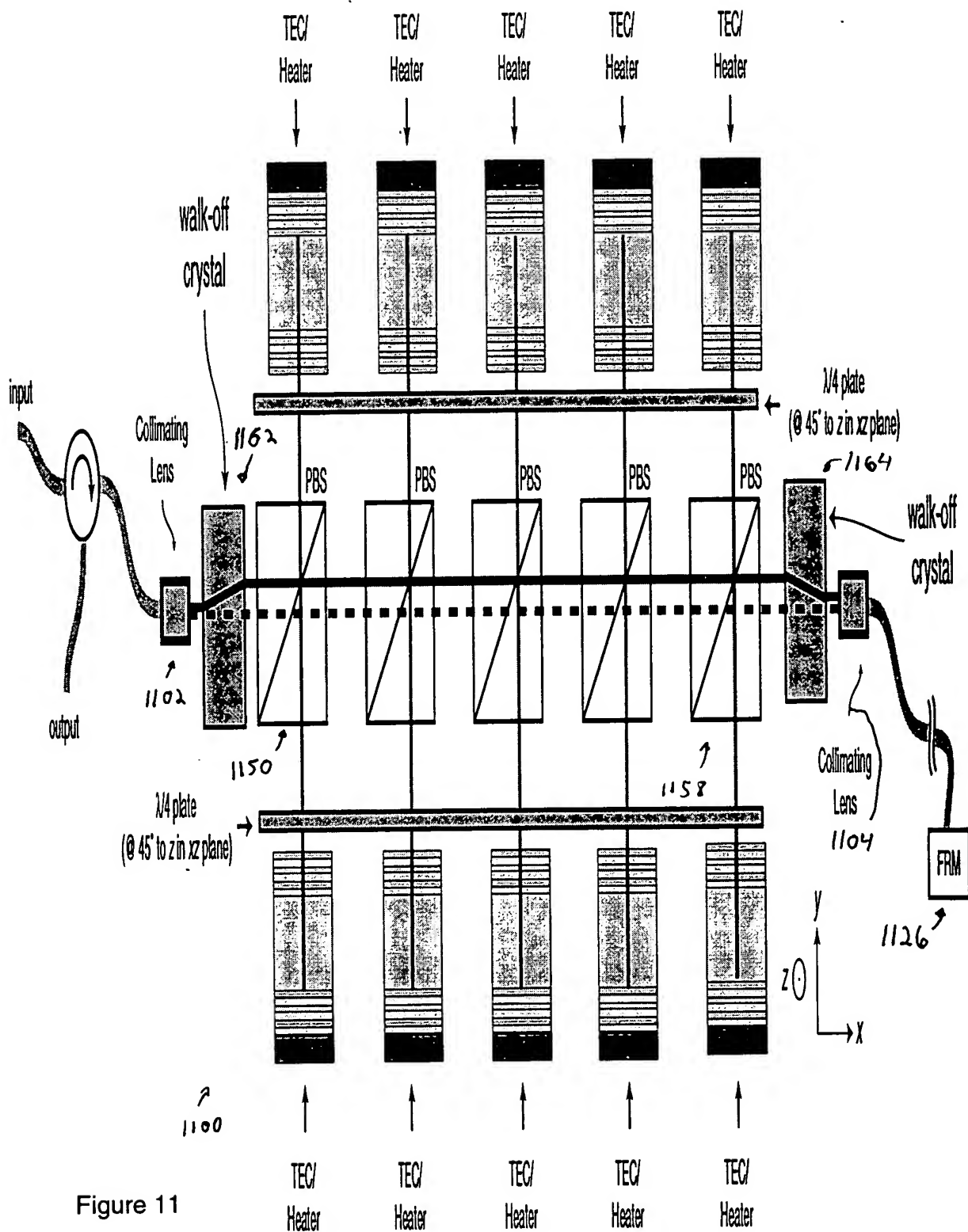


Figure 11

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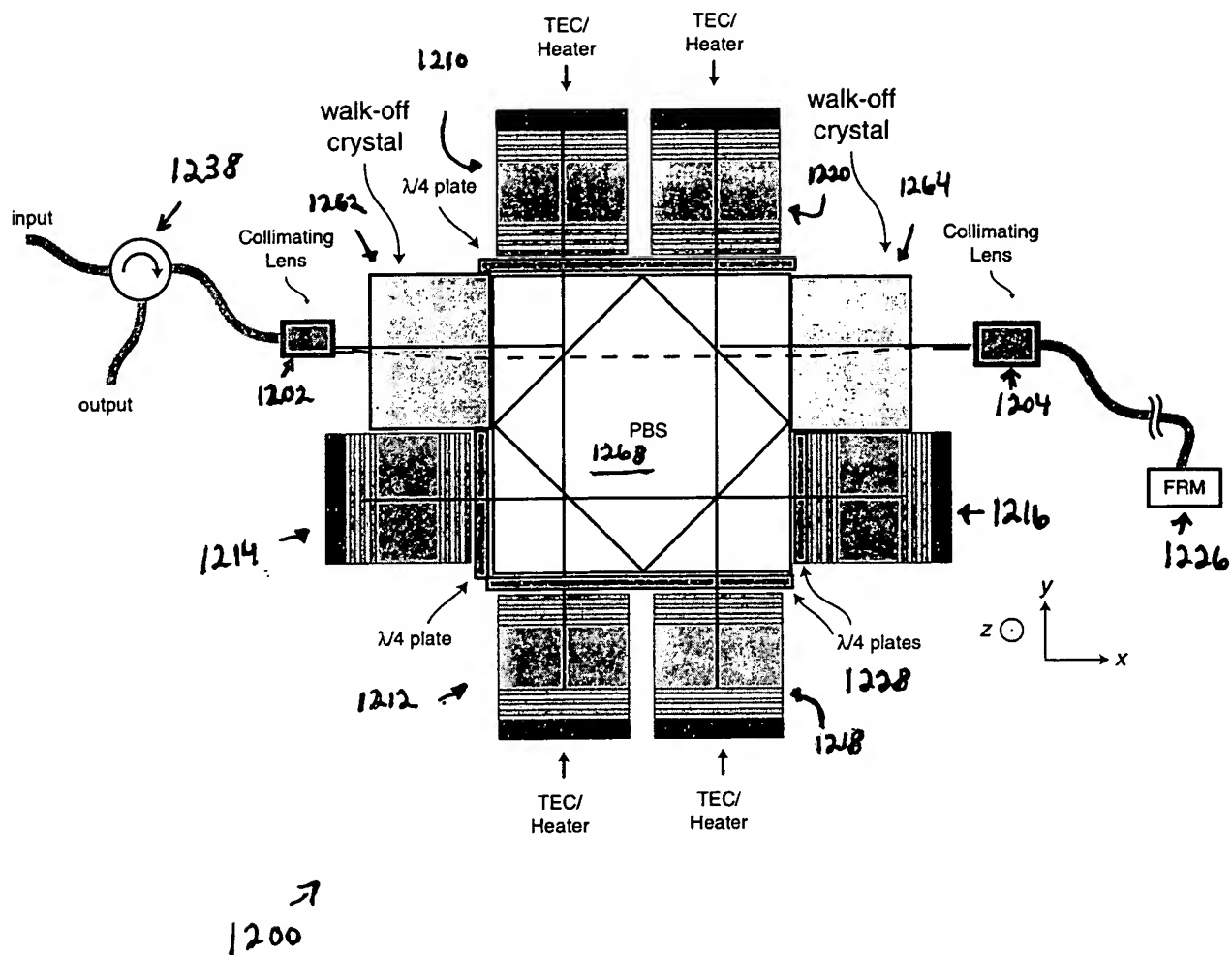


Figure 12

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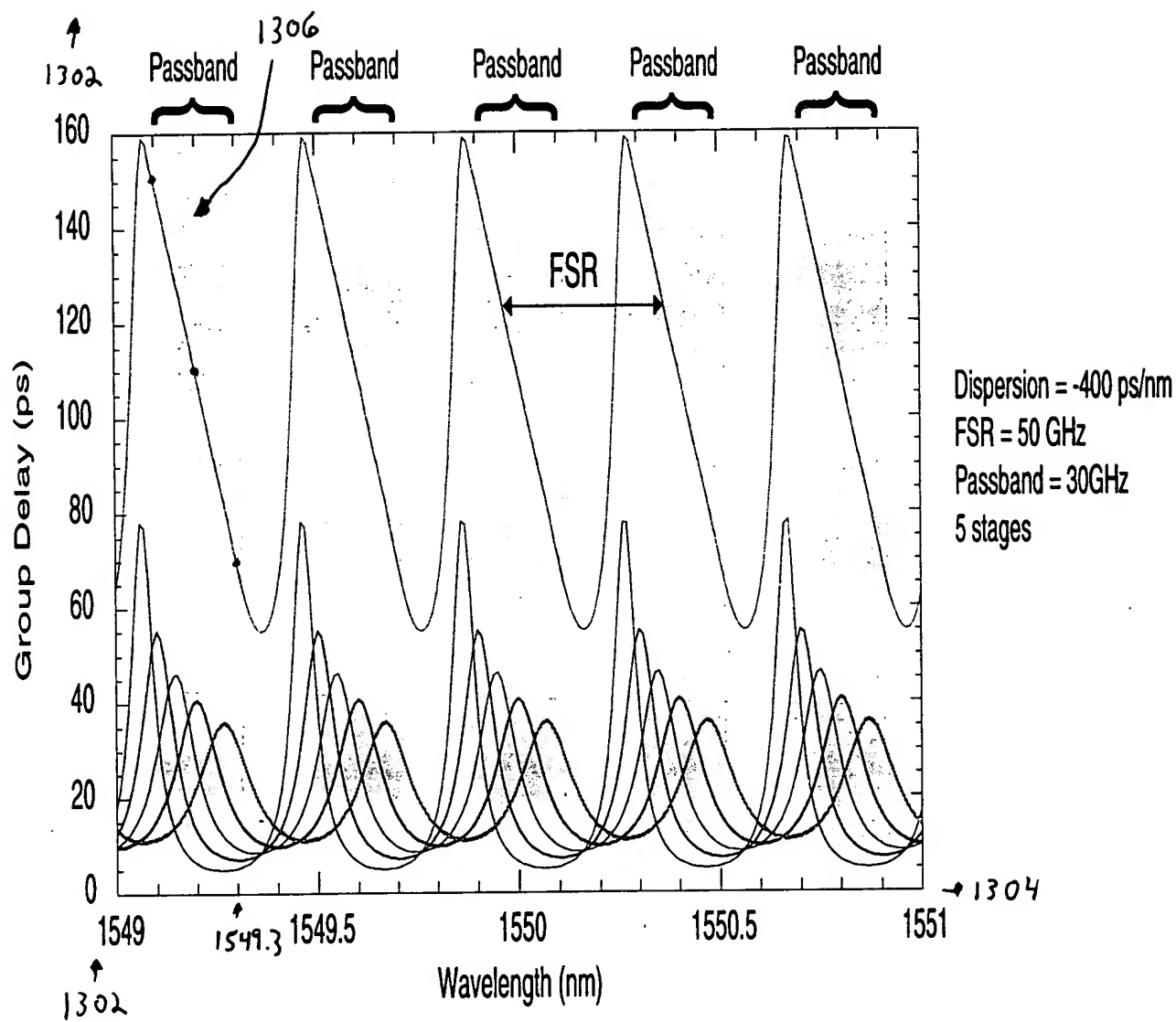


Figure 13

1300

10071445-020602

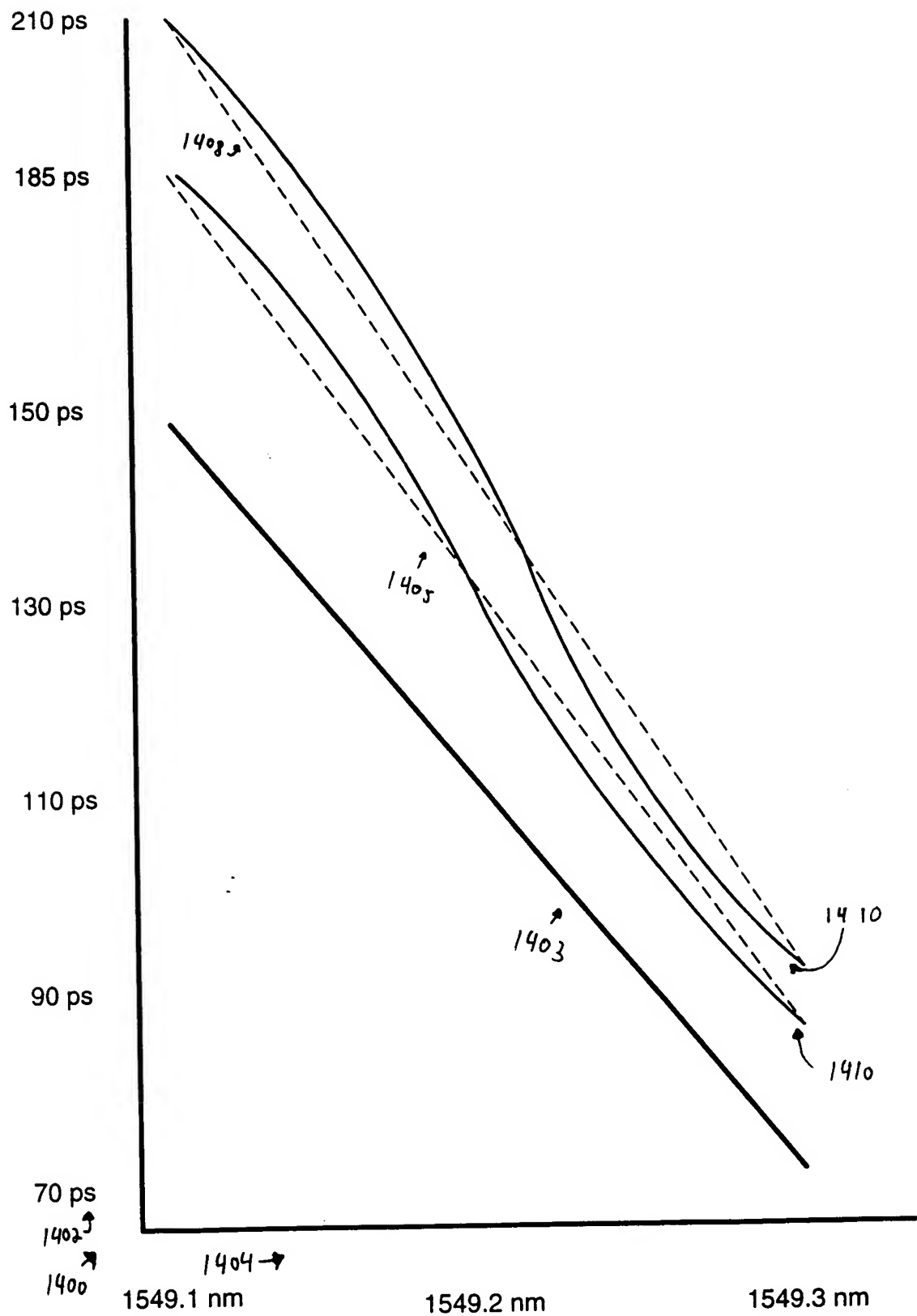


Figure 14

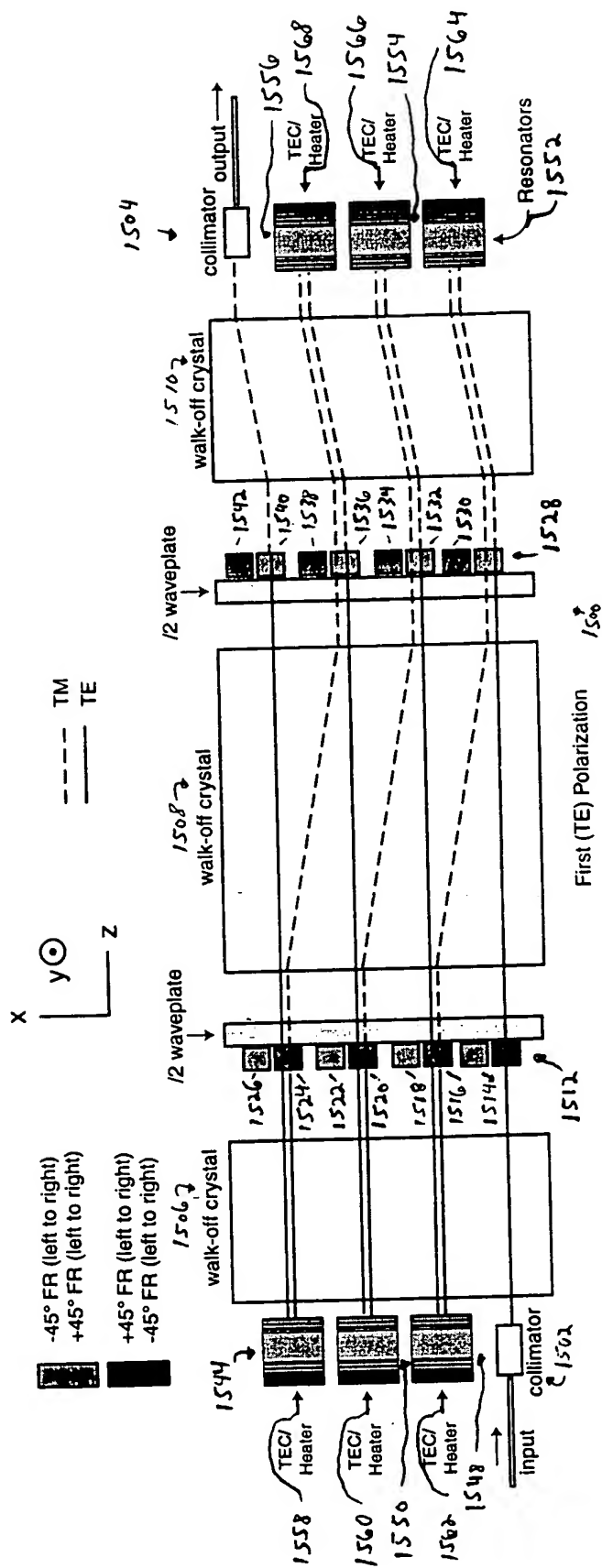
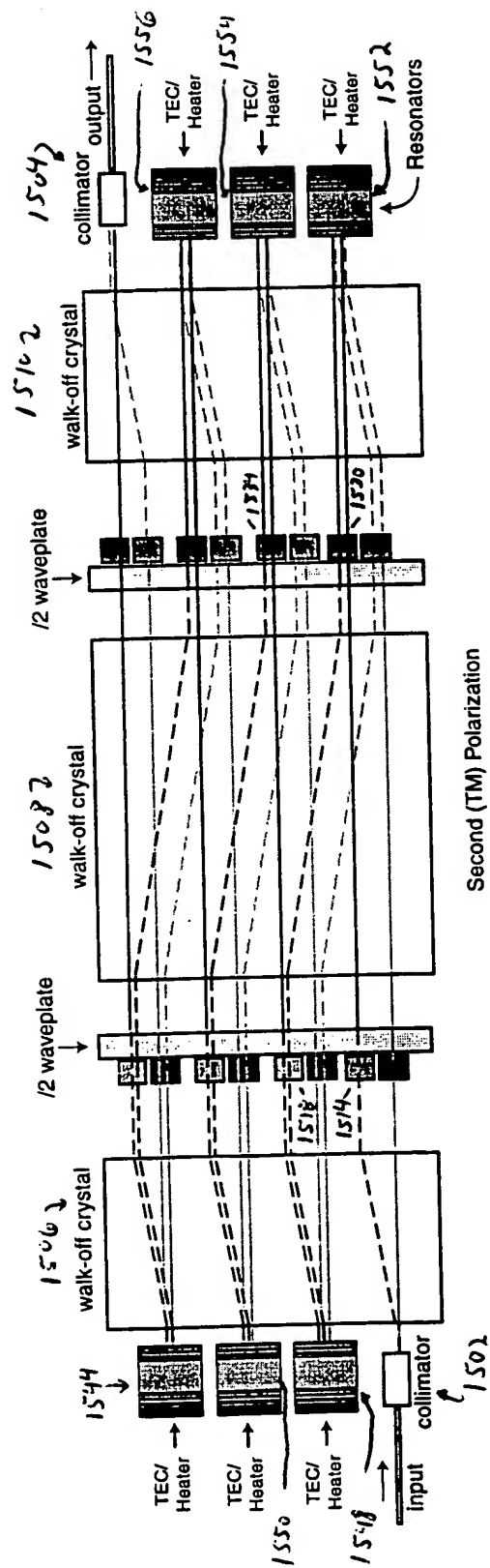


Figure 15



Second (TM) Polarization
Figure 16